

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An apparatus comprising:
 - first control means for routing a functional clock to a functional unit within an integrated circuit;
 - second control means for routing a scan clock to the functional unit, the second control means being independent of the first control means, wherein the first and second control means enables testing of the functional unit while other functional units not being tested operate using the functional clock.
2. (Original) The apparatus of claim 1 wherein the second control means comprises a cluster test controller, a unit test controller, and a local test clock controller coupled to each other in a logical hierarchy to control the functional unit independently of any other functional unit.
3. (Original) The apparatus of claim 2 wherein the functional unit comprises a plurality of FUBs.
4. (Original) The apparatus of claim 3 further comprising a third clock means for at least partially controlling the plurality of FUBs independently of the functional clock.
5. (Original) The apparatus of claim 4 wherein the third clock means comprises a master clock generation circuit and a slave clock generation circuit.
6. (Original) The apparatus of claim 5 wherein the first control means is a hierarchy of functional clocks to control the functional unit during normal operation.

7. (Original) The apparatus of claim 6 wherein the second control means is a hierarchy of functional clocks to control the functional unit during testing.
8. (Original) A processor comprising:
 - a functional clock hierarchy to operate a plurality of functional units within the processor at a first set of clock speeds;
 - a scan clock hierarchy to operate the plurality of functional units with the processor at a second set of clock speeds independently of the functional clock hierarchy, the second set of clock speeds being slower than the first set of clock speeds.
9. (Original) The processor of claim 8 wherein the scan clock hierarchy comprises integrated test control (ITC) logic, cluster test control (CTC) logic, unit test control (UTC) logic, and local test clock control (LTCC) logic coupled to each other in a logical hierarchy in order to help operate the plurality of functional units independently of other functional units.
10. (Original) The processor of claim 9 wherein the ITC logic, CTC logic, the UTC logic, and the LTCC logic comprise registers to control the routing of a functional clock and a scan clock from the pins of the processor to the plurality of functional units.
11. (Original) The processor of claim 10 wherein the ITC logic controls the routing of the functional clock independently of the routing of the scan clock to the CTC logic.

12. (Original) The processor of claim 11 wherein the CTC logic controls the routing of the functional clock independently of the routing of the scan clock to the UTC logic.
13. (Original) The processor of claim 12 wherein the UTC logic controls the routing of the functional clock independently of the routing of the scan clock to the LTCC logic.
14. (Original) The processor of claim 13 wherein the LTCC logic controls a master and slave clock that operate independently of the scan clock and functional clock.
15. (Original) The processor of claim 14 wherein the master and slave clocks control testing of a FUB.
16. (Original) The processor claim 15 wherein the registers enable a first set of functional units to operate at the functional clock speed concurrently with a second set of functional units operating at the scan clock speed without the first or second set of functional units experiencing delay caused by the operation of the other.
17. (Original) The processor of claim 16 wherein the scan clock hierarchy is to be used during testing of the processor.
18. (Currently Amended) A system comprising:
 - a memory unit;
 - a processor coupled to the memory unit and the audio device, the processor comprising a scan control chain and a functional

control chain to route a scan control clock and a functional control clock, respectively, to a plurality of functional units and operate a first set of the plurality of functional units independently and concurrently with a second set of the plurality of functional units.

19. (Original) The system of claim 18 wherein the scan control clock is able to control the plurality of functional units without experiencing delay caused by the functional control clock and visa versa.
20. (Original) The system of claim 19 wherein the scan clock chain is to pass data relating to an automatic test pattern between an automatic test pattern generator and one of the first and second set of functional units.
21. (Original) The system of claim 20 wherein the processor comprises a scan clock enable signal to enable the scan clock chain independently of the functional clock chain.
22. (Original) The system of claim 21 wherein the processor comprises a plurality of inputs to receive scan data generated from the automatic test pattern generator.
23. (Original) The system of claim 22 wherein the processor comprises a plurality of outputs to deliver scan data to testing apparatus.
24. (Original) The system of claim 23 wherein the number of the plurality of inputs and the number of the plurality of outputs is 36.

25. (Previously Presented) The system of claim 24 wherein the scan clock is able to operate at a slower speed than the functional clock without either incurring a delay due to the other.
26. (Previously Presented) An apparatus comprising:
 - a functional clock chain to operate a plurality of functional units within the processor at a first set of clock speeds;
 - a scan clock chain to operate the plurality of functional units with the processor at a second set of clock speeds independently of the functional clock chain, the second set of clock speeds being slower than the first set of clock speeds;
 - an integrated test control (ITC) logic, cluster test control (CTC) logic, unit test control (UTC) logic, and local test clock control (LTCC) logic coupled to each other in a logical hierarchy in order to help operate the plurality of functional units independently of other functional units, wherein the ITC logic, CTC logic, the UTC logic, and the LTCC logic comprise registers to control the routing of a functional clock and a scan clock from the pins of the processor to the plurality of functional units.
27. (Original) The apparatus of claim 26 wherein the ITC logic controls the routing of the functional clock independently of the routing of the scan clock to the CTC logic.
28. (Original) The apparatus of claim 27 wherein the CTC logic controls the routing of the functional clock independently of the routing of the scan clock to

the UTC logic.

29. (Original) The apparatus of claim 28 wherein the UTC logic controls the routing of the functional clock independently of the routing of the scan clock to the LTCC logic.
30. (Original) The apparatus of claim 29 wherein the LTCC logic controls a master and slave clock that operate independently of the scan clock and functional clock.
31. (Original) The apparatus of claim 30, wherein the master and slave clocks control testing of a FUB.
32. (New) A processor comprising:
 - a first clock circuit to clock a first functional unit while the first functional unit is not being tested;
 - a second clock circuit to clock a second functional unit independently of the first clock circuit while the second functional unit is being tested.
33. (New) The processor of claim 32 wherein the second clock circuit comprises a cluster test controller, a unit test controller, and a local test clock controller.
34. (New) The processor of claim 33 wherein the functional unit comprises a plurality of functional units.
35. (New) The processor of claim 34 further comprising a third clock circuit to at least partially control the plurality of functional units independently of the

functional clock circuit.

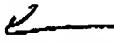
36. (New) The processor of claim 35 wherein the third clock circuit comprises a master clock generation unit and a slave clock generation unit.
37. (New) The processor of claim 36 wherein the first clock circuit is to couple a functional clock signal to the first and second functional units during normal operation of the first and second functional units.
38. (New) The processor of claim 37 wherein the second clock circuit is to couple a functional clock signal to the first and second functional units during testing of the first and second functional units.

If there are additional fees due, please charge them to our Deposit Account No. 02-2666.

Respectfully submitted,

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